Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application using (Original) (Currently Amended) (New) (Canceled) nomenclature, as recited in the below listing of claims.

1. (Currently Amended) A timing recovery loop for generating adjusted timing pulses from a baseband signal waveform encoding a self clocking digital bit stream, the timing recovery loop comprising,

a pulse detector for generating data transition pulses from the baseband signal waveform, the pulse detector for comparing the data transition pulses with the adjusted timing pulses for generating ~~early~~ lead signals and lag signals, the lead signals and lag signals being generated from the data transition pulses occurring within a window period of time referenced to the adjusted timing pulses, the data transition pulses corresponding to respective data bits of the self clocking digital bit stream with each of the data bits having a bit period, the data transition pulses being synchronized to the baseband waveform,

a random walk counter for counting the early signals and lag signals over a plurality of bit periods for generating a running count, the ~~early~~ lead signals and lag signals being generated when the data transition pulses lead and lag the adjusted timing pulses,

a threshold comparator for determining when the running count exceeds a predetermined first threshold count value, and

a timing pulse delay adjustor for adjusting an adjusted timing pulse delay communicated to the pulse detector for delaying the adjusted timing pulses for synchronizing the adjusted timing pulses

with the data transition pulses and with the baseband signal over a plurality of bit periods when the running count exceeds the predetermined threshold count value.

2. (Original) The timing recovery loop of claim 1 further comprising,

a data detector for generating a reconstructed digital bit stream by sampling the baseband signal waveform by the adjusted timing pulses.

3. (Previously Presented) The timing recovery loop of claim 1 further comprising,

a threshold count value selector for selecting the first threshold count value.

4. (Previously Presented) The timing recovery loop of claim 1 further comprising,

a threshold count value selector for selecting the first threshold count value, and

an adaptive means for monitoring the rate at which the timing pulse delay is adjusted, the threshold value count selector adaptively selecting different first threshold count values when the adjustment rate exceeds a predetermined rate being a second threshold count value.

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5. (Previously Presented) The timing recovery loop of claim 1 further comprising,

a count magnitude generator for generating the magnitude count from the running count, the magnitude count being fed to the threshold count comparator for determining when the running count exceeds the predetermined first threshold count value, and

a count sign clipper for generating a count sign from the running count, the count sign being fed to the timing pulse delay adjustor for generating a timing pulse delay to adjust the adjusted timing pulses, the sign count for increasing the timing pulse delay when the data transition pulses arrive late relative to the adjusted timing pulses and for decreasing the timing pulse delay when the data transition pulses arrive early relative to the adjusted timing pulses.

6. (Original) The timing recovery loop of claim 1 wherein the pulse detector comprises,

a data transition pulse generator for generating the data transition pulses,

a timing delay for delaying reference timing pulses into the adjusted timing pulses, and

a lead and lag generator for generating lead and lag signals for early and late arrivals of the data transition pulses relative to the adjusted timing pulses.

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7. (Original) The timing recovery loop of claim 1 wherein the pulse detector comprises,

a data transition pulse generator for generating the data transition pulses,

a timing delay for delaying reference timing pulses into the adjusted timing pulses,

a data transition pulse counter for counting the number of data transition pulses within a search window following an adjusted timing pulse, and

a lead and lag generator for generating lead and lag signals for early and late arrivals of the data transition pulses relative to the adjusted timing pulses when one and only one data transition pulse occurs within each search window following an adjusted timing pulse.

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8. (Original) The timing recovery loop of claim 1 wherein the pulse detector comprises,

a data transition pulse generator for generating the data transition pulses,

a window delay for delaying the data transition pulses by half of a search window to center the data transition pulses within respective search windows,

a timing delay for delaying by a timing pulse delay the reference timing pulses into the adjusted timing pulses, the timing pulse delay being generated by the timing delay adjustor, the timing pulse delay being adjusted when the running count exceeds predetermined threshold value,

a data transition pulse counter for counting the number of data transition pulses within the search window following an adjusted timing pulse, and

a lead and lag generator for generating lead and lag signals for early and late arrivals of the data transition pulses relative to the adjusted timing pulses when one and only one data transition pulse occurs within a respective one of the search windows following a respective one of the adjusted timing pulses.

9. (Previously Presented) The timing recovery loop of claim 1, wherein,

the random walk counter sums the lead signals and lag signals as the running count.

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10. (Currently Amended) A timing recovery loop for generating adjusted timing pulses from a baseband signal waveform having zero crossings and encoding a self clocking digital bit stream, the timing recovery loop comprising,

a pulse detector for generating data transition pulses from the zero crossings of the baseband signal waveform, the pulse detector for comparing the data transition pulses with the adjusted timing pulses for generating ~~early~~ lead signals and lag signals, the lead signals and lag signals being generated from the data transition pulses occurring within a window period of time referenced to the adjusted timing pulses, the data transition pulses corresponding to respective data bits of the self clocking digital bit stream with each of the data bits having a bit period, the data transition pulses being synchronized to the baseband waveform,

a random walk counter for counting the ~~early~~ lead signals and lag signals over a plurality of bit periods for generating a running count, the ~~early~~ lead signals and lag signals being generated when the data transition pulses lead and lag the adjusted timing pulses,

a threshold comparator for determining when the running count exceeds a predetermined first threshold count value, and

a timing pulse delay adjustor for adjusting an adjusted timing pulse delay communicated to the pulse detector for delaying the adjusted timing pulses for synchronizing the adjusted timing pulses with the data transition pulses and with the baseband signal over a plurality of bit periods when the running count exceeds the predetermined threshold count value.

11. (Previously Presented) The timing recovery loop of claim 10 wherein,

the baseband waveform signal having zero crossings encodes the digital bit stream using a modulation method selected from the group consisting of BPSK, QPSK, GMSK, 16-QAM, and 64-QAM.

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